General Description

Arrive G.Fast Switch Codechip provides two uplink ports up to 10 Gb/s and four G.999.1 ports at rate of up to 2.5 Gb/s. The FPGA-based SoC solution and external front-end devices can help quickly to make quick-to-market distribution point equipment, specifically for Fiber-to-the-Distribution-Point (FTTdp) or to bring gigabit speeds to multiple dwelling unit (MDU) applications in access networks.

Arrive's CodeChips are provided in fully complete bitstream format or encrypted netlist format along with firmware device driver/software API packages, BSP, schematic and layout reference design files, design reviews, board testing and support from initial project definition to mass production. The CodeChip bitstreams and encrypted netlists are targeted to specific FPGA devices that are selected based on the mix of features requested and customer preference.

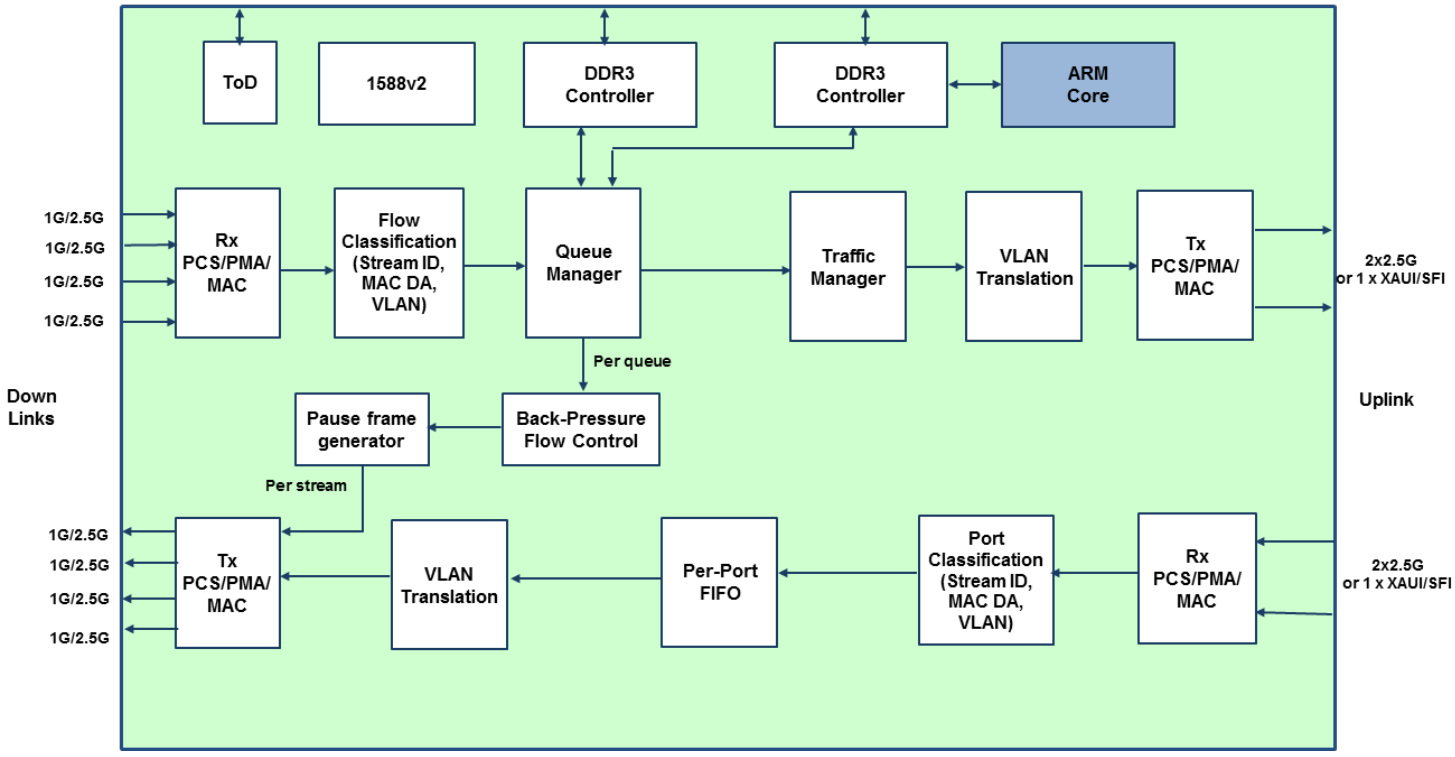
Key Features

- A low-cost, low-power-consumption, FPGA-based G.Fast Switch core with a single application specific high-level API software driver for all CodeChip variants. Supports protocol stack handling
- Uplinks: 2 * 1G/2.5G/10G Ethernet
- Downlinks: Up to 4 * 1G/2.5G Ethernet, each supporting up to 16 users in G.999.1 connectivity
- Provides integrated multi-core CPU by using FPGA-based SoC devices
- Very low-cost DDR3 for large buffers
- L2+ packet classification
- VLAN translation
- Advanced operation and maintenance (OAM) support
- Network time synchronization with IEEE 1588v2
- Available on low-cost FPGA (supplied by customer)

Applications

- G.Fast/DSL broadband distribution point units

Block Diagram



Features Summary

Interfaces

- Uplinks: 2*1G/2.5G/10G Ethernet Interface
- Downlinks: 4 * 1G/2.5G GbE. Each downlink has up to16 users in G.999.1 connectivity
- WAN-PLL/ToD/1PPS Timing Interface

Classification

- Support flow classification based on stream ID, MAC DA, VLAN, and port ID in the direction of downlink to uplink. Each field can be optional
- QoS classification based on VLAN CoS and Flow ID in the direction of downlink to uplink
- Downlink destination port look up, based on MAC DA and VLAN in the direction of uplink to downlink
- MAC DA and VLAN learning/aging
- IGMP snooping multicast replication
- 1K entries (MAC + VLAN) database
- 1K flows/stream IDs support

QoS

- Up to 128 queues based on flow ID and QoS in the direction of downlink to uplink
- Shaping and Scheduling (SP, DWRR, SP+DWRR) supported in the direction of downlink to uplink
- Per-downlink port FIFO used for the direction of uplink to downlink
- Back-pressure mechanism
- Per-queue back-pressure
- External DDR3 Memory for packet buffer
- Per-stream ID pause-frame generation (G.999.1 and 802.1Qbb)

VLAN Translation

- 1:1/N:1 VLAN translation

OAM

- Ethernet Link OAM (EFM)
- 802.1ag/Y.1731 service OAM
- Hardware acceleration engine, co-operate with software to reduce CPU load
- 64 MIPs/MEPs
- MIP/MEP classification base on port/VLAN
- CCM/LBM/LBR/LTM/LTR

IEEE 1588v2

- Ordinary Clock (OC)/ Boundary Clock (BC) mode
- Transparent Clock (TC) mode

Software Support

- APIs with C-language source code release
- Ethernet Link OAM (EFM)
- Service OAM
- 1588v2 servo-algorithm

Sales and Support Contacts

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A listing of our products, including data sheets and basic product specs, is available on Arrive's website.

